Floating Point Inverse Square Root

February 2025 Product Specification

InverseSquareRootCore Facts

- **Design File Formats:** VHDL
- **Verification:** Test Bench
- **Instantiation Templates:** VHDL
- **Simulation Tool Used:** Vivado Simulator (XSIM)
- **Support Provided by:** Barzak

Features

- Available under terms of the Barzak IP License
- IEEE-754 compatible (accurate to 1 ULP but does not support full IEEE-754 rounding modes. Supports only round to zero)
- Single-precision real format support
- 5-stage pipelined architecture
- Accuracy 1 ULP
- Results available every clock cycle
- Fully configurable and synthesizable
- Implemented using Harmonized Parabolic Synthesis for optimal accuracy
- Supports normalized numbers, NaN and infinity

Example Implementation Statistics for Xilinx FPGA

Family	Example device	Fmax(Mhz)	LUT	FF	DSP	BRAM
Zynq Ultrascale	XCZU7EV-3	260.213	192	163	14	1.5

Architecture Overview

- **5 stage pipeline unit:** The computational unit is divided into five stages. Each stage is set by the divided computational formula of Harmonized Parabolic Synthesis.

Core I/O Signals

Signal	Direction	Description
clk	Input	Global system clock
datai[31:0]	Input	32-bit input data bus
datao[31:0]	Output	32-bit output data bus

Applications

- Math coprocessors
- DSP algorithms
- Embedded arithmetic processing
- Real-time signal processing
- Computer graphics

Verification Methods

The Barzak Inverse Square Root core has been verified in simulation using fully automated testbenches. The inverse square root result is evaluated for 2^{23}(8,388,608) inputs (every conceivable mantissa value).

Additionally, verification was performed using an FPGA testing board, comparing computed inverse square root results with a PC-based IEEE-754 floating-point processor.

Related Information

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